CLAIMS

We claim:

1. An integrated circuit device comprising:

an integrated circuit substrate;

a conductive lower electrode layer of a Metal-Insulator-Metal (MIM) capacitor on the integrated circuit substrate;

a dielectric layer on the lower electrode layer;

a conductive upper electrode layer of the MIM capacitor on the dielectric layer;

a first intermetal dielectric layer on the upper electrode layer, the first intermetal dielectric layer including at least one via hole extending to the upper electrode layer;

a first conductive interconnection layer on the at least one via hole of the first intermetal dielectric layer;

a second intermetal dielectric layer on the first intermetal dielectric layer, the second intermetal dielectric layer including at least one via hole extending to the first conductive interconnection layer and at least partially exposing the at least one via hole of the first intermetal dielectric layer; and

a second conductive interconnection layer on the at least one via hole of the second intermetal dielectric layer that electrically contacts the first conductive interconnection layer.

2. The device of Claim 1 wherein the first conductive interconnection layer comprises a landing pad type independent interconnection layer that connects the second conductive interconnection layer to the upper electrode.

3. The device of Claim 1 wherein the dielectric layer has a thickness between the lower electrode layer and the upper electrode layer greater than the thickness of the dielectric layer in other regions of the device.

4. The device of Claim 1 wherein the lower electrode layer is electrically coupled to an impurity region of the integrated circuit substrate.

5. The device of Claim 1 wherein the first intermetal dielectric layer further comprises an insulating pattern formed only on the upper electrode.

6. The device of Claim 1 wherein the at least one via hole of the first intermetal dielectric layer comprises a plurality of via holes separated from each other.

7. The device of Claim 2 wherein the landing pad type interconnection layer is formed to the same height as the first intermetal dielectric layer.

8. The device of Claim 2 wherein the landing pad type interconnection layer comprises a plurality of interconnections separated from each other.

9. The device of Claim 3 wherein the thickness of the dielectric layer in the other regions is from about 0.01 μm to about 0.1μm.

10. The device of Claim 1 wherein the first interlevel dielectric layer further comprises a trench formed with a greater diameter than that of the first via hole and to a smaller depth than that of the first via hole.

11. The device of Claim 1 further comprising a transistor having a source, a drain and a gate formed on the integrated circuit substrate and wherein the lower electrode layer of the MIM capacitor is electrically coupled to the drain of the transistor.

12. The device of Claim 11 further comprising a second transistor having a drain and a gate formed on the integrated circuit substrate, the second transistor having a common source with the first transistor and the drain of the second transistor being electrically coupled to the second interconnection layer.

13. The device of Claim 5 wherein the insulating pattern is selected from the group consisting of an oxide layer, a nitride layer, an fluorine-doped silicate glass (FSG) layer, an organo silicate glass (OSG) layer, a silicon carbide (SiC) layer and combinations thereof.

14. A semiconductor device, comprising:

an MIM capacitor formed on a semiconductor substrate, the MIM capacitor including a lower electrode, a dielectric layer on said lower electrode, and an upper electrode on said dielectric layer;

a first intermetal dielectric formed on the upper electrode of the MIM capacitor, the first intermetal dielectric having a first via hole on the upper electrode of the MIM capacitor;

a landing pad type independent interconnection layer formed on the first via hole;

a second intermetal dielectric having a second via hole exposing the landing pad type independent interconnection layer formed on the MIM capacitor; and

an interconnection layer formed on the second via hole, the interconnection layer connected to the upper electrode of the MIM capacitor via the landing pad type independent interconnection layer.

15. The device of Claim 14, wherein the lower electrode of the MIM capacitor is electrically coupled to a drain formed in the semiconductor substrate.

16. The device of Claim 14, wherein the thickness of the dielectric layer formed under the upper electrode is greater than that of the dielectric layer formed at regions other than the region where the upper electrode is formed.

17. The device of Claim 16, wherein the thickness of the dielectric layer formed at the regions other than the region where the upper electrode is formed ranges from 0.01 to 0.1μm.

18. The device of Claim 14, wherein an insulating pattern is formed on the upper electrode and is formed of one of an oxide layer, a nitride layer, an FSG layer, an OSG layer, and an SiC layer, or a combination thereof.

19. The device of Claim 18, wherein the insulating pattern is not formed at the regions other than the region where the upper electrode is formed.

20. The device of Claim 14, wherein the landing pad type independent interconnection layer is formed to the same height as the first intermetal dielectric.

21. The device of Claim 14, wherein the interconnection layer connected to the upper electrode of the MIM capacitor is formed to the same height as the second intermetal dielectric.

22. The device of Claim 14, wherein the landing pad type independent interconnection layer is formed of a plurality of interconnections which are separated from each other.

23. A semiconductor device, comprising:

a lower electrode of an MIM capacitor formed on a semiconductor substrate and coupled to an impurity region formed in the semiconductor substrate;

a dielectric layer formed on the lower electrode;

an upper electrode of the MIM capacitor formed on the dielectric layer;

an insulating pattern formed on the upper electrode of the MIM capacitor;

a first intermetal dielectric formed on the insulating pattern, the first intermetal dielectric having a first via hole exposing the upper electrode of the MIM capacitor;

a landing pad type independent interconnection layer formed on the first via hole;

a second intermetal dielectric having a second via hole exposing the landing pad type independent interconnection layer formed on the MIM capacitor; and

an interconnection layer formed on the second via hole, the interconnection layer coupled to the upper electrode of the MIM capacitor via the landing pad type independent interconnection layer.

24. The device of Claim 23, wherein the thickness of the dielectric layer formed under the upper electrode of the MIM capacitor is greater than that of the dielectric layer formed at regions other than the region where the upper electrode is formed.

25. The device of Claim 23, wherein the thickness of the dielectric layer formed at the regions other than the region where the upper electrode is formed ranges from 0.01 to 0.1μm.

26. The device of Claim 23, wherein an insulating pattern formed on the upper electrode is formed of one of an oxide layer, a nitride layer, an FSG layer, an OSG layer, and an SiC layer, or a combination thereof.

27. The device of Claim 23, wherein the landing pad type independent interconnection layer is formed of a plurality of interconnections which are separated from each other.

28. A semiconductor device comprising:

a lower electrode of an MIM capacitor formed on a semiconductor substrate, the lower electrode electrically coupled to an impurity region formed in the semiconductor substrate;

a dielectric layer formed on the semiconductor substrate including the lower electrode, wherein the dielectric layer has a thickness between the lower electrode and an upper electrode of the MIM capacitor greater than the thickness of the dielectric layer in other regions of the device;

the upper electrode of the MIM capacitor formed at the region where the dielectric layer is thick;

an insulating pattern formed on the upper electrode of the MIM capacitor;

a first intermetal dielectric formed on the insulating pattern, the first intermetal dielectric having a first via hole on the upper electrode of the MIM capacitor;

a landing pad type independent interconnection layer formed on the first via hole;

a second intermetal dielectric having a second via hole exposing the landing pad type independent interconnection layer formed on the MIM capacitor; and

an interconnection layer formed on the second via hole, the interconnection layer connected to the upper electrode of the MIM capacitor via the landing pad type independent interconnection layer.

29. The device of Claim 28, wherein the thickness of the dielectric layer formed at the regions other than the region where the upper electrode is formed ranges from 0.01 to 0.1μm.

30. The device of Claim 28, wherein the landing pad type independent interconnection layer is formed of a plurality of interconnections which are separated from each other.

31. A semiconductor device comprising:

transistors having a common source region and a drain region respectively,

a first insulating layer formed on the transistors and having a plurality of contact holes filled with conductive patterns coupled to the drain regions;

a second insulating layer formed on the first insulating layer having a plurality of first via holes;

a lower electrode of a MIM capacitor formed on the second insulating layer and electrically coupled to one of the drain regions through one of the first via holes in the second insulating layer;

a first interconnecting layer formed on the second insulating layer and electrically coupled to one of the drain regions through one of the first via holes in the second insulating layer;

an upper electrode of a MIM capacitor formed over the lower electrode of the MIM capacitor;

a dielectric layer formed on the lower electrode of the MIM capacitor and the second insulating layer, wherein the dielectric layer between the lower electrode layer and the upper electrode layer is thicker than the thickness of the dielectric layer in other regions of the device;

an insulating pattern formed on the upper electrode of the MIM capacitor;

a first intermetal dielectric layer formed on the insulating pattern and the dielectric layer, the first intermetal dielectric layer having a second via hole on the interconnecting layer and a third via hole on the upper electrode of the MIM capacitor and;

a landing pad type independent interconnection layer formed on the third via hole;

a second interconnection layer formed on the second via hole;

a second intermetal dielectric having a fourth via holes exposing the landing pad type independent interconnection layer formed on the MIM capacitor and the second interconnection layer; and

a third interconnection layer formed on the third via hole, the interconnection layer connected to the upper electrode of the MIM capacitor via the landing pad type independent interconnection layer.